IN THE SPECIFICATION:

Amend the title as shown:

~~METHOD AND STRUCTURE OF VERTICAL STRAINED SILICON DEVICES~~

Structure of Vertical Strained Silicon Devices

Amend paragraph 40 as shown:

[0040] Figure 7 shows the transistor area, denoted generally with numeral 150 and having the result of forming gate dielectric 152, e.g., thermally grown oxide, on layer 134, filling the remaining aperture with conducting material 154 and then optionally etching the outer portion of the top of the conducting material 155 to form apertures 156. The conducting material 154 is preferred to be polysilicon.

Amend paragraph 47 as shown:

[0047] The spacing ~~182~~ 183 between the gate contact for the illustrated cell and the passing wordline on the right is set by the groundrules. For a given groundrule, therefore, the increase in trench width caused by the consumption of silicon reduced the space

available for the bitline contact for the trench, which has to be outside the trench and not contacting the passing wordline 177.